

PATENT
SZS&Z Ref. No. : IO031111PUS
Atty. Dkt. No. INFN/SZ0032

REMARKS

This is intended as a full and complete response to the Office Action dated September 29, 2005, having a shortened statutory period for response set to expire on December 29, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 11-15, 17 and 20-23 are pending in the application and remain pending following entry of this response. New claim 24 has been added to recite aspects of the invention and does not introduce new matter.

Claim Rejections - 35 USC § 102

Claims 11-15, 17 and 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by *Ogawa* (U.S. Patent No. 5,321,662). Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Ogawa* does not disclose "each and every element as set forth in the claim". For example, *Ogawa* does not disclose monitoring write operations by a memory controller, as recited in independent claims 11 and 20, and performing refresh operations for only those rows containing cells involved in monitored write operations. In contrast, portions of *Ogawa* cited by the Examiner (Column 3, lines 35-44) teach that:

...it is presumed that memory cells of all rows (for example 256 rows) in the memory cell array are refreshed by an externally requested refresh operation (for example, a CBR refresh) within term Tec...

Further, from the Summary (Column 4, lines 28-35), even when an external refresh is not provided during a predetermined time length:

...the short refresh time refresh circuit refreshes all the memory cells in the memory cell array in a predetermined short time....

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Thus, *Ogawa* does not teach refreshing only those rows that have been written to, as recited in claims 11 and 20, but teaches refreshing all rows of memory cells.

Similarly, *Ogawa* is silent as to *any one of* row state circuitry configured to maintain a plurality of bits indicative of rows that are to be refreshed, interface circuitry configured to receive the plurality of bits from a memory controller and to transfer the plurality of bits to the row state circuitry, and refresh enable circuitry configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry, as recited in independent claim 13. As described above, *Ogawa* provides no teaching of limiting the number of rows that are refreshed but, rather teaches refreshing all rows. Further, the Examiner fails to indicate any portion of *Ogawa* that teaches interface circuitry, as recited in the claimed.

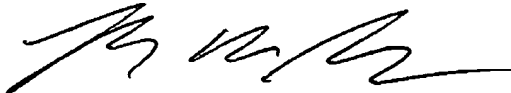
Therefore, the claims are believed to be in condition for allowance, and allowance of the claims is respectfully requested.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,



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